a2 cont'd.

image, but operates with a conventional overhead projector (OHP) having a light source and projection optics, to project the display image onto a display screen. Examples of such LCD projectors and LCD projection panels are sold under the respective trademarks LITEPRO and PANELBOOK by In Focus Systems, Inc. of Wilsonville, Ore., the assignee of the present application.

a3

The paragraph at column 2, lines 5~~4~~17, is amended as follows:

Because the LCD used in multimedia display systems [require] requires digital video signals, either the LCD or the system normally has an analog to digital (A/D) signal converter for converting the PC-generated analog video signals into a digital format suitable for driving the LCD. The A/D signal converter is usually combined with a phase-locked loop (PLL), which may comprise a phase comparator, a low-pass loop filter, and a voltage-controlled oscillator (VCO) formed in a loop to generate a feedback signal that locks into H_{sync}. In order to generate a selected multiple *n* of clock pulses for each period of H_{sync}, a divide-by-*n* counter is added to the feedback loop between the VCO output and the phase comparator.

a4

The paragraph at column 2, lines 50-54, is amended as follows:

The stream of digitized values [form] forms the digital video data signal, which is addressed to the LCD to appropriately set LCD pixels at blank (black) or selected activated (non-black) status to replicate the image defined by the analog video signal.

a5

The paragraph at column 2, line 61 - column 3, line 21 is amended as follows:

Referring to the analog video signal 1 and pixel clock signal 4' in FIG. 1*b*, tracking error results from the number *n* of pixel clocks being improperly set. As discussed above, the number *n* of pixel clocks should be equal to the number of pixel data components 2 of each horizontal line of

analog video data signal. In FIG. 1*b*, the proper setting of *n* results in the pixel data components 2 not being sampled at a consistent point. For instance, *n* is set too large in clock signal 4' (i.e. the clock signal frequency is too high). The resulting crowding of the pixel clock pulses 5' yields an additive leftward drift of the pixel clock pulses 5' relative to the pixel data components 2 of the analog video data signal 1. Such drift causes sampling in the transition regions 3. For instance, as indicated by positional bracket A, the leading edges 7' of the third through the sixth clock pulses 5' sample in transition zones 3 of the analog video signal 1. Accordingly, the transition zone data will be erroneous, and the image information from adjacent non-sampled pixel data components 2 will be missing from the digitized video signal. If *n* is erroneously set large enough, the pixel clock pulses may be so [crowed] crowded that individual analog pixel data components 2 may be double-sampled. On the other hand, if *n* is set too small, (i.e. the pixel clock signal frequency is too low), the dispersion of the pixel clock pulses results in a rightward drift wherein sampling may also occur in the transition regions. In all of these cases, the erroneous sampling provides erroneous video signal data that may degrade the LCD image quality.

a5 cont'd.

The paragraph at column 3, lines 44-48, is amended as follows:

a6

Thus, in light of these disadvantages, it is a [principle] principal object of the present invention to provide an apparatus and a method for producing a digital video signal from [a] an analog video signal that automatically corrects phase and tracking errors.

The paragraph at column 3, lines 53-56, is amended as follows:

a7

It is another object of the present invention to provide an apparatus and a method for producing a digital video signal from [a] an analog video signal that automatically corrects the horizontal position of a video image on the display object.

The paragraph at column 6, lines 54-67, is amended as follows:

The operation of the preferred embodiment will now be explained. The display system 10 determines the resolution mode by a firmware program that uses the mode identification counter 43. H_{sync} is input through conductor 45 to the mode identification counter 43, and the number of 50 MHz counter clocks over twenty H_{sync} pulses is counted. In this way, an average number of clocks per line is obtained. V_{sync} is input through conductor 47 into the mode identification counter 43, and the number of lines for each V_{sync} pulse is obtained. The firmware then accesses a look-up table that determines resolution based on the number of 50 [Mhz] MHz clocks per twenty lines, and number of lines per frame. An exemplary look-up table showing a few common non-interlaced 60 Hz video modes is as follows:

a8

171 173

The two paragraphs at column 9, lines 1-26, are amended as follows:

Once the actual width W is determined, the microcontroller compares it with the expected width E. If E=W, then the clock phase and the number *n* of clocks per line is correct. In other words, at E=W, each [discreet] discrete data region (plateau) of the analog video data signal is aligned with and sampled by a pixel clock, resulting in error-free digitization of the analog video data signal. In this case, *n* and the pixel clock phase are left unchanged for the scanning of the next frame.

171 173

If W>E+1 or W<E, then the number *n* of clocks per line is incorrectly set, resulting in tracking error. To correct such tracking error, [a] the number *n* of pixel clocks is adjusted to a new number $n'=n\cdot(E/W)$. The original *n* is replaced by the adjusted *n'*, and the next frame is scanned as set forth above. Such adjustment of *n* is iteratively repeated every frame until W=E or W=E+1. Put another way, if the actual width W is larger than the expected width E, the number of pixel clocks *n* per line is decreased, (i.e. the period of each pixel clock is increased, and the frequency of the pixel clock signal is decreased), so that the width of the E pixel clocks is effectively spread out to precisely register with the active pixel data region.

a9

171 173

A

a9 cont'd.

Conversely, if the actual width W is smaller than the expected width E, the number of pixel clocks *n* per line is increased, so that the width of the E pixel clocks is effectively contracted to register precisely with the active pixel data region of the analog video data signal.

The paragraph at column 9, line 66 - column 10, line 7 is amended as follows:

a10

It is also noteworthy that the method and apparatus of the present invention can be used to properly horizontally position the active video region 11 (FIG. 1*d*) on the LCD. In this application, the value of LEFT STATUS may be used to determine when video data begins to be stored by the WRAM 132. Thus, no data is stored for the blanked margins on either side of the active video region, eliminating the [possible] possibility that spuriously activated analog pixel components in the blanked margin region will be transferred to the LCD.

In the Drawings:

Amend Figs. 1a, 1b, 1c, 1d, and 2 as indicated in red ink on the enclosed copies of these drawing figures.

In the Claims:

Amend claim 1 as follows:

a11

1. (Amended) A method for recovering a correct phase and frequency clock for an analog video signal that is converted for display on a digital display object having pixels arranged in lines and columns, the analog video signal including an analog video data signal that is operable for raster scanning in lines across a CRT screen to form consecutive frames of video information, the raster scanning controlled by timing signals that control a line scan rate and a frame refresh rate, to produce consecutive frames of video information, comprising the steps of:

converting an analog video signal to a digital video signal;

estimating an expected width of an image producible by the analog video signal;